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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/722,593

11/28/2003

Pascal Gabet

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EXAMINER

LE, DINH THANH

ART UNIT

PAPER NUMBER

2816

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

03/01/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/722,593	Applicant(s) GABET ET AL.	
	Examiner DINH T. LE	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 December 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2 and 4-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2 and 4-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

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NON-FINAL REJECTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/5/06 has been entered.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 1-2 and 4-9 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, the “Na” and Nb” on lines 10-11 is confusing because it is unclear if these are additional “Na” and “Nb” or further recitation “Na” and “Nb” on lines 3-4.

The remaining claims are dependent from the above rejected claims and therefore also considered indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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Claims 10-11 and 13-16 are rejected under 35 USC 102 (b) as being anticipated by Petersson et al (US 5,140,284).

As the best construed, Petersson et al disclose in Figure 1 a circuit comprising:

- a synthesizer (21-25) for synthesizing a frequency (25-1 12.5M1c) with a variable steps (j7.5M1Z- 25M1'17,=12.5M1V to 112.5M1-12-75M1R=37.5M114, see Table 1 at column 5;
- one variable rank divider (26) located after the synthesizer (221-25); and
- a frequency controller (31) for deliver division rank command to the divider (26), the frequency command to the divider (2 1) for controlling the variable frequency steps and the synthesis command to the divider (25) for controlling the synthesis steps.
- With regard to claim 11, the variable-rank divider Nb vary according to an arithmetic sequence.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 4-9, 12 and 17 are rejected under 35 USC 103(a) as being unpatentable over Petersson et al (US 5,140,284) in view and Figure 2 of the applicant's admitted prior art and further in view of Dekker (US 6,239,660).

Petersson et al discloses a synthesizer circuit

As the best construed, Petersson et al disclose in Figure 1 a circuit comprising:

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- a synthesizer (21-25) for synthesizing a frequency (25-112.5MHZ) with a variable steps (37.5MHZ- 25MHZ=12.5MHZ to 112.5MHZ-75MHZ=37.5MHZ), see Table 1 at column 5;
- one variable rank divider (26) located after the synthesizer (221-25); and
- a frequency controller (31) for deliver division rank command to the diver (26), the frequency command to the divider (21) for controlling the variable frequency steps and the synthesis command to the divider (25) for controlling the synthesis steps.

However, Petersson et al does not disclose that the synthesizer is a fractional step phase-locked loop synthesizer and a filter is placed after the divider.

The applicant's admitted prior art teaches in Figure 2 a synthesizer comprising a fractional step modulo for providing fractional frequency steps.

Dekker teaches in Figure 2 a synthesizer circuit comprising a filter (212) placed after the synthesizer (200) for removing unwanted high frequency noise.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the fractional step modulo taught by the admitted prior art in the circuit of Petersson et al for the purpose of providing fractional frequency steps and the filter taught by Dekker in the circuit of Petersson for the purpose of removing unwanted high frequency noise.

With regard to claim 4, the variable-rank divider N_b takes the values $N_1=8$ to $N_p=24$, these values following an arithmetic progression, and wherein the maximum frequency of the synthesizer is given by $F_4=8 \times 4.68 \text{M}11\text{Z}=37.5 \text{M}14\text{Z}$.

With regard to claims 6 and 8, the variable-rank divider (26) takes the values $N_1=8$ to $N_p=24$.

With regard to claim 7 and 14, $173:=12.5 \text{M}1-12$ is substantially equal to or smaller than

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$a_{174} = 8/12 \times 37.5M + 1Z = 25M11Z$ where $a = 8/12$ is the smallest value obtained in dividing two consecutive elements one after the other.

With regard to claim 9, as understood, the mixer is read on the phase detector (22) of Petersson et al where it receives the output signal (fvco) and a mixing signal (fre).

With regard to claims 5 and 12, although the step frequency $F3 = 12.5\text{MHz}$ is not equal or slightly lower than $(N1/N2) \times F4 = 8/24 \times 37.5\text{MHz} = 25\text{MHz}$ as claimed; however, the step frequency of Petersson et al can be selected by selecting the divisors P and R as shown on Table 1 at column 5. Thus, selecting a predetermined frequency step for the circuit of Petersson in order to accommodate with the requirement of a predetermined system in which the circuit of Petersson is to be used would have been obvious at the time of the invention. The same is true for claim 17 in which the reference frequency and the step frequency can be selected to equal to the LCM of the sequence N1.

Response to Applicant's Arguments

The applicant argues that the present invention allows faster switching time and lower phase noise and lower spurious lines than those of Petersson in view of Deckker. The arguments are not persuasive because these arguments are based on limitations not being recited in the rejected claims. There is nothing stated in the rejected claims about faster switching time, lower phase noise and lower spurious lines.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner

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should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/27/07



DINH T. LE
PRIMARY EXAMINER